SOLID-STATE SWITCHING MODULATOR R&D FOR KLYSTRON

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Abstract
KEK has two programs to improve reliability, energy efficiency and costs of klystron modulators. The first is to improve a line-type modulator by use of a solid-state switch that can be used instead of thyratoron. We have developed a solid-state switch which consists of 15 SI-thyristors stacked in series. The switch has been successfully operated at 45 kV hold-off voltage, 6000 A peak current, 6 μs pulse-width and 25 Hz. The second program is to develop a new hybrid modulator with numbers of individual solid-state pulse modulators which are stacked in a voltage-adder configuration for the Japan Linear Collider(JLC). To study this type of modulator, a ten-stage test modulator has been built and successfully tested.

1. INTRODUCTION

The power efficiency, reliability and costs of the klystron modulators are extremely important. their improvements are a major challenge in a large scale linear collider such as the JLC[1]. We have improved the performance of klystron modulators using a solid-state technology. In this paper, we will describe the solid-state switch development for a line-type modulator, and the JLC modulator design and the experimental results of the test modulator.

2. SOLID-STATE SWITCH DEVELOPMENT

To improve the reliability of the line-type of modulator, we have developed a solid-state switch to replace the thyratron tubes. The solid-state switch has been designed and built using SI-thyristors and tested with a line-type modulator.

2.1 45kV Solid-State Switch

2.1.1 Switching devices

The Static Induction SI-thyristror is suitable for the switch device because of its high-power handling and fast turn-on capabilities. We have investigated the NGK RT103N 4 kV reverse conducting SI-thyristor(including a freewheeling diode within a press-pack ceramic housing). To evaluate the performance of this device, the fast turn-on characteristics of five-stack of SI-thyristor which was connected in series were studied in a very low-inductance circuit. By using a coaxial structure, the residual inductance was successfully reduced to less than 136 nH. When an anode voltage of 15 kV was applied, a maximum peak current of 10 kA, dI/dt of 110 kA/μs, and switching time of 128 ns were obtained. The switching time is the time required for the anode voltage to decrease to 10% of its maximum value. It was confirmed that the turn-on characteristics of the SI-thyristors are comparable to the thyratorns.

2.1.2 Switch assembly

A simplified circuit diagram of the solid-state switch is shown in Fig. 1. Each circuit card assembly consists of a SI-thyristor, a resister capacitor network, break-over diodes and a gate-driving circuit. The break-over diodes protect the devices whenever the voltage across the circuit card assembly exceeds the rated voltage of the diodes. This method protects the stacks from over-

voltages that would result in the destruction of all the devices. Both the trigger and power cables for each card were isolated from high-voltage through ferrite core transformers.

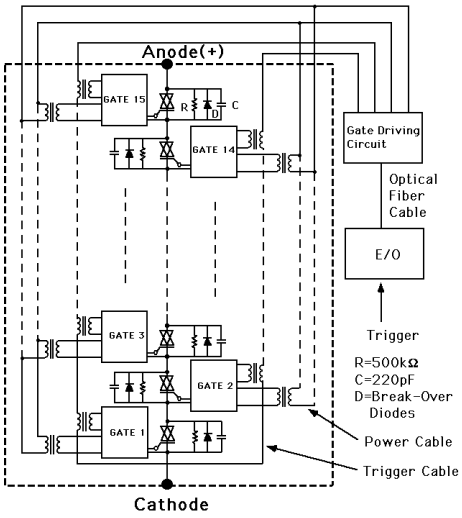

Fig. 1 Simplified circuit diagram of 45kV Solid-State Switch.

Table 1

45 kV Solid-State Switch Specifications

Device	SI-thyristor NGK:RT103N(4kV)
Series Connection	15 devices
Insulation	Oil
Cooling	Forced oil cooling
Size	Cylindrical type 550 mm x 300 mm

The SI-thyristors are normally-on type devices. To make a hold-off state, a bias voltage of –10 V is applied between the gate and cathode electrodes. To make a hold-on state, a pulse with a voltage of 160 V is applied. The performance of the gate circuit influences the fast turn-on characteristics. As a fast switch for the gate pulse, a specially designed low inductance MOSFET unit is used. The maximum gate current reaches 200 A during switching. The gate circuit is implemented in the closest possible proximity of the device to reduce the total inductance.

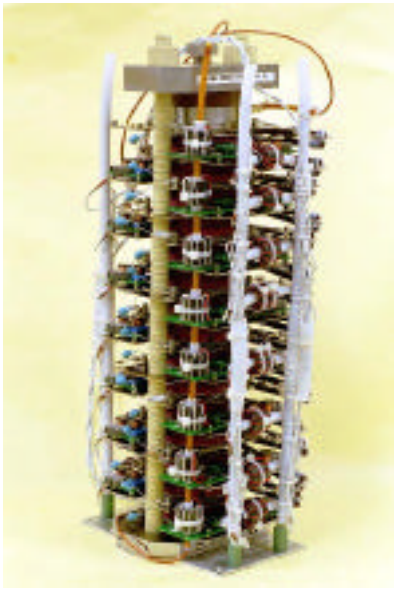

Fig. 2(a) 45 kV Solid-State switch assembly

Fig. 2(b) Gate driving circuit and SI-thyristor.

The stack assembly and SI-thyristor with gate circuit are shown in Figs. 2(a) and 2(b). The stacked devices are housed in a single cylindrical tank with a diameter of 300 mm and a height of 550 mm. The tank is filled with oil for insulation and cooling of the internal devices.

2.2 Test Results

2.2.1 Test circuit

The performance of the solid-state switch was studied with a line-type 5045 klystron modulater at KEK Accelerator Test Facility, ATF. Figure 3 shows the circuit diagram of the modulator. The klystron modulator consists of a high-voltage charging power supply, PFNs, a solid-state switch and a conventional 1:15 pulse transformer. The inverter power supply charges the PFNs up to 45 kV with a charging time of 19 ms. After a hold time of 5 ms, the switch is triggered and the output pulse is applied to the SLAC 5045 Klystron. The anode voltage of the switch was measured with a Iwatsu's high-voltge probe (model HV-60) and the anode current of the switch was measured with a Pearson's current transformer (model 3025) which was inserted in a return line of the PFNs.

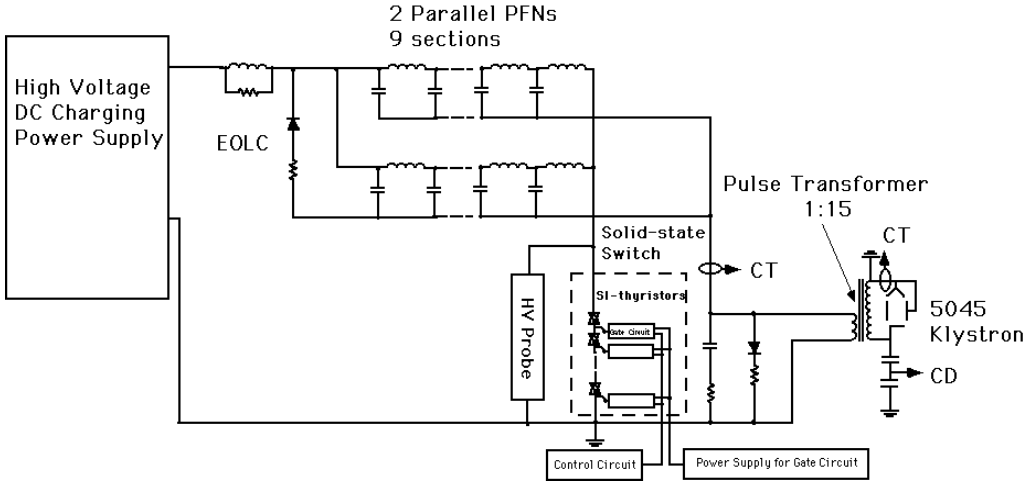

Fig. 3 Simplified circuit diagram of the klystron modulator.

The test was made at 25 Hz, limited by the charging capability of the inverter power supply. Figure 4 gives the typical switch voltage and current waveforms at a PFN voltage of 45 kV. A peak current of 6000 A, di/dt of 10 kA/μs and a pulse-width of 6 μs were obtained.

2.2.2 Switching waveform

To compare this solid-state switch to a thyratron switch, the Marconi CX1536 thyratron switch was also tried in the modulator. Figure 5 shows the typical switch voltage and the current waveforms of the thyratron switch at a PFN voltage of 45 kV. The measured switching times of the solid-state and thyratron switches were 208 ns and 40 ns, respectively. While the rise time of the thyratron switch was five times faster than the solid-state switch. The rise time of both the switch currents was similar, because it is limited by the time constant of the output circuit including the pulse transformer. However, it is shown that the switching loss of the solid-state switch is higher than the thyratron, because of the difference of the switching time.

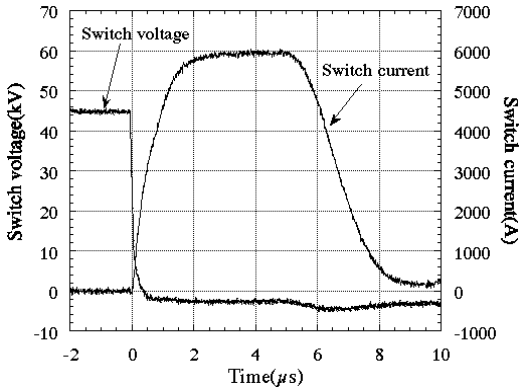

Fig. 4 Switch voltage and current waveforms with the solid-state switch.

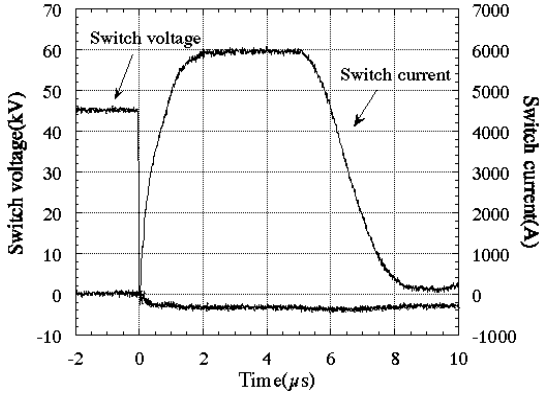

Fig. 5 Switch voltage and current waveforms with the thyratron switch.

Figure 6 shows the klystron voltage and current waveforms at a PFN voltage of 45 kV with the solid-state switch. A peak current of 376 A, a peak voltage of 361 kV and a pulse-width of 6 μs were obtained. The pulses with a peak power of 136 MW were switched by the solid-state switch.

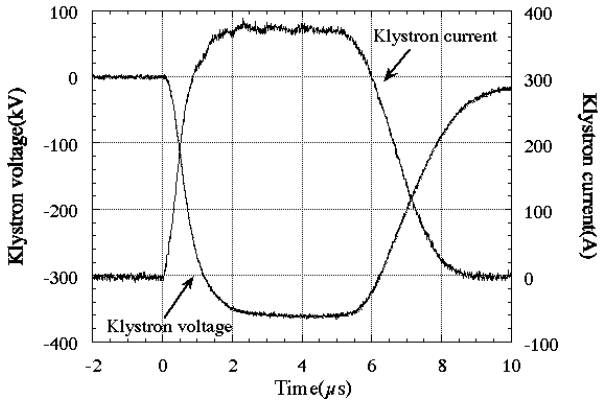

Fig. 6 Klystron voltage and current waveforms with the solid-state switch.

2.2.3 Switch losses

The switch losses were measured by calorimetry which is a reliable method. A cooling system of the solid-state switch is a simple closed-loop system consisting of a oil tank, a pump, a flowmeter and a radiator. The pump has a rated delivery of 4.7 l/min. The temperatures of both the inlet and the outlet of the tank were always monitored and recorded by a pen recorder during operation. Therefore, the switch losses can be calculated from their temperature differences and the flow rate of the cooling oil. In this system, the temperature difference of 1°C corresponds to a switch power loss of 130 W. The switch losses were measured at a PFN voltage of 20, 30, 40 and 45 kV. The results are summarized in Table 2. At a PFN voltage of 45 kV, the temperature difference between the inlet and outlet was measured to be 8.5°C, which corresponds to a switch loss of 1.1 kW. It is also found that the switch loss is proportional to the stored energy in the PFN.

Table 2
Switch losses versus PFN voltage

PFN voltage (kV)	PFN Stored energy (J/pulse)	Switch losses (J/pulse)	Details of switch losses		
			Balance resisters (J/pulse)	Gate circuits (J/pulse)	Devices (J/pulse)
20	162	9.4(5.8%)	0.98(10.5%)	0.8(8.5%)	7.6(81.0%)
30	365	21.3(5.8%)	1.92(9.0%)	0.8 (3.8%)	18.6(87.2%)
40	648	32.8(5.1%)	2.77(8.5%)	0.8(2.4%)	29.2(89.1%)
45	820	41.1(5.0%)	3.10(7.4%)	0.8(2.4%)	37.2(90.7%)

A value in parentheses of switch losses column shows the ratio of energy to the PFN stored energy. A value in parentheses in details of switch losses column shows the ratio of each loss energy to switch losses.

The switch losses take place in balance resisters, gate circuits and devices. The losses in the balance resisters are calculated from ohmic loss during the PFN charging. The losses of the gate circuits are calculated from the measured current and voltage of power line supplied to them. By subtracting these contributions from the measured switch losses, the losses in the devices are obtained. It is found to be 41 J/pulse at 45 kV. This value corresponds to 5% of the total PFN stored energy, with about 90% of this loss dissipated in devices themselves. Therefore, these switches still need to be improved to further reduce losses. However, it has been confirmed that 45 kV solid-state switch has a switching capability comparable to a thyratron.

2.2.4 Future program

The main problem at the initial stage of the performance test was a failure of device break-down which was found when the klystron broke down in 45 kV PFN operation. In order to investigate this failure, we have inspected the devices and performed a break-down experiment using a model stack. From this investigation, it was found that the SI-Thyristor is damaged when the reverse current exceeds 4 kA. To protect the devices, the reverse diodes will be connected to the solid-state switch in parallel. To investigate the long-term reliability of the modified switch, it will be installed and operated in the modulator to collect lifetime data. The SI-thyristor will be also improved to reduce the turn-on and conduction losses.

3. HYBRID MODULATOR FOR JLC

We are developing a new hybrid modulator with numbers of pulse generator stages in series and a pulse transformer for the JLC. To study the modulator of this type, we have built a ten-stage test modulator and performed a preliminary test.

3.1 Modulator Design

The klystron modulator for the JLC is required to produce a 500 kV, 530 A, 1.5 μs flat-top pulse to drive a pair of 75 MW PPM-klystrons[3]. Table 2 shows the specifications of the JLC klystron modulator. The JLC hybrid modulator uses multiple solid-state modulators(cell-modulators) which are stacked in a voltage-adder configuration and a 1:5 primary split pulse transformer. Figure 7 shows the basic circuit diagram of the JLC klystron modulator. Each cell-modulator is a direct switching modulator which is capable of generating a 2 kV pulse at 2650 A. Some cell-modulators are used as a waveform control modulator to obtain output waveform with a wide flat-top. The modulator unit, which consists of 26 cell-modulators(operating at 2 kV per cell) stacked in series and which generates a 50 kV pulse at 2650 A, drives one of the primary circuits of the pulse transformer. The other unit also drives the other primary circuit. The pulse transformer provides the klystrons with a 500 kV pulse. The inverter charging system provides a DC power to each cell-modulator.

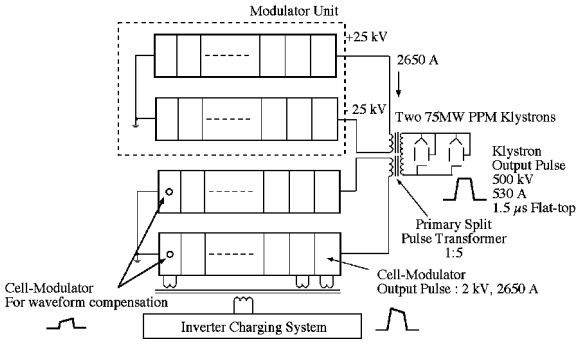

Fig. 7 Basic circuit diagram of JLC Klystron Modulator.

Table 2
Specifications of JLC Klystron Modulator

Parameter	Value
Peak Klystron voltage	500 kV
Total peak current	530 A
Flat-top Pulse Duration	1.5 μs
Pulse top flatness	2%
Energy Efficiency(Goal)	70%
Repetition rate	150 Hz

3.2 Cell-Modulator

A unit of the cell-modulator consists of an energy storage capacitor, a solid-state switch which turns on and off the circuit. It also includes a bypass diode which protects the solid-state switch and isolates the circuit from all other stages. The cell-modulator works as follows. The capacitor is initially charged through a charging transformer. When the switch is turned off as shown in Fig. 8(a), the cell-modulator is completely separated from output circuit, and the output current flows through the bypass diode. When the switch is turned on as shown in Fig. 8(b), the current in the diode is commutated. The energy storage capacitor is now connected in series with output circuit, and the charging voltage of the energy storage capacitor is added in the output circuit. Both the pulse width and timing of the output pulse of the cell-modulator is determined by controlling the gate trigger of the switch.

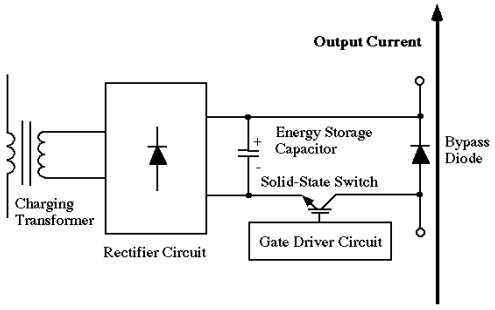

Fig. 8(a) Cell-modulator when the switch is turned off.

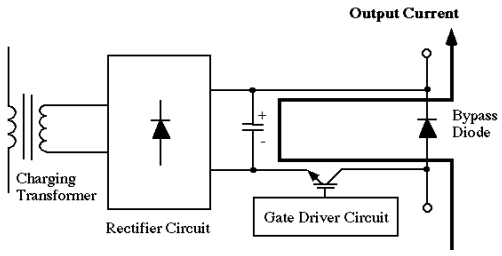

Fig. 8(b) Cell-modulator when the switch is turned on.

3.3 10-stage Test Modulator

3.3.1 Circuit

Figure 9 shows the circuit diagram of a 10-stage test modulator. It consists of 10 cell-modulators which are stacked in series, a charging system to provide a DC power to each cell modulator, and a resistor load. The design parameters of the test modulator are shown in Table 3. A photograph of the stack assembly with a resistor load is shown in Fig. 10.

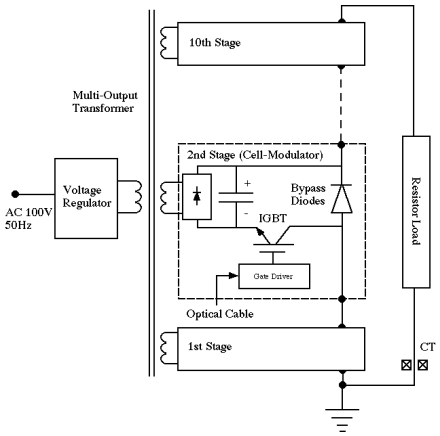

Fig. 9 Simplified Schematic of 10-stage Test Modulator Circuit.

Table 3
Main parameters of 10-stage test modulator

Parameter	**Value**
Output Voltage	20 kV
Output Current	2.7 kA
Pulse Width	3 μs
Number of Cell-Modulator	10 stages
Repetition Rate	5 Hz

A photograph of a cell-modulator is shown in Fig. 11. An Insulated Gate Bipolar Transisitor(IGBT), MITSUBISHI CM1200HB-66H was used as a solid-state switch. The CM1200HB-66H is rated at 3.3 kV peak voltage and 1200 A average current. The gate drive circuit for each IGBT receives its trigger pulses from a trigger control circuit through optical cables. The capacitance of the energy storage capacitor was determined to be 17.3 μF in order to keep its voltage drop within 10%. The capacitor of each cell-modulator is charged through a multi-output transformer. The output voltage of the modulator is regulated by adjusting the charging voltage of each cell-modulator. The output current of the modulator was measured with a Pearson's current transformer.

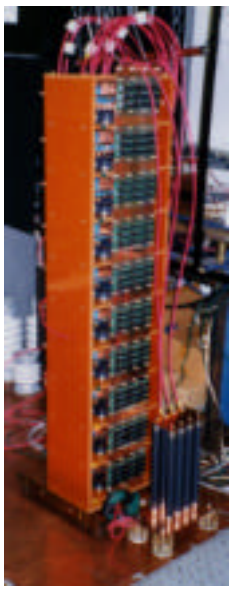

Fig. 10 10-Stage Test Modulator.

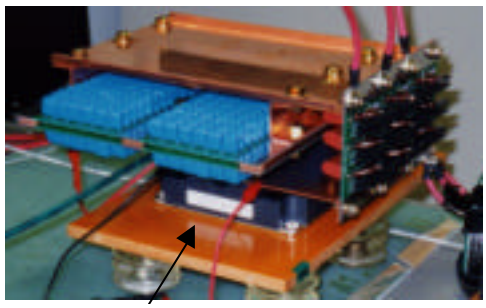

Fig. 11 A Cell-Modulator.

3.3.2 Output waveform[4]

Figure 12 shows an example of the waveform of the output current through the 5.5 Ω resistor load. In this test, only 6 stages were used and each stage operated at a voltage of 2 kV. A pulse with a peak voltage of 12 kV, a peak current of 2160 A , a rise time(10-90%) of 630 ns and a fall time(10-90%) of 450 ns was successfully generated. The output pulse has a droop of approximately 10%, which is consistent with the expected droop in the energy storage capacitor.

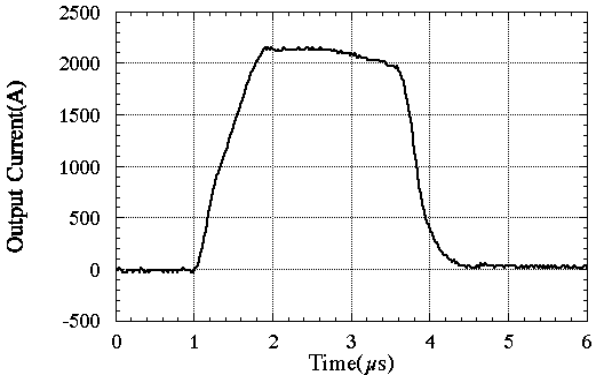

Fig. 12 Output current waveform.

3.3.3 Waveform Control

We have tried to control the output waveform with appropriate triggering of cell-modulators. In this test, a set of 10 cell-modulators(stages) was operated at a voltage of 1 kV with a 4.1 Ω resistor load. The first and second stages were used as a waveform compensation modulator. In order to obtain the maximum flat-top width, the trigger timings for the first and second stages were adjusted. Figure 13 shows the trigger timing for each stage. Figure 14 shows the output current waveform at the resistor load, with and without waveform compensation. The output waveform without compensation was drooped with no flat-top but the compensated waveform became rectangular with a wide flat-top. From this result, we found that individual trigger control for cell-modulator enables us to produce excellent waveform with a wide flat-top and it improves a power efficiency.

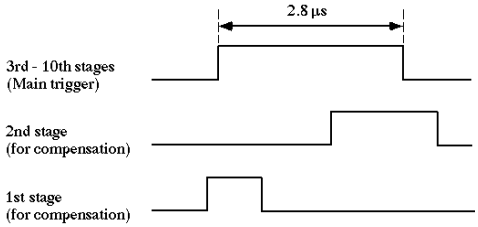

Fig. 13 Trigger timing chart.

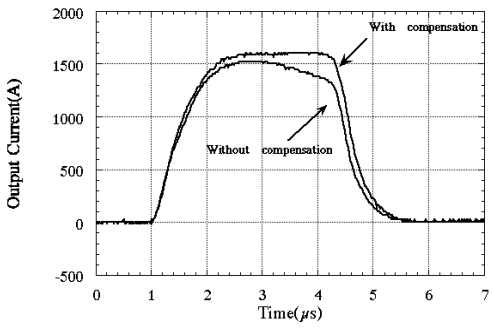

Fig. 14 Output current waveforms with and without compensation.

3.4 Future program

Testing of the 10-stage test modulator has just stated. Full power testing with a peak voltage of 20 kV and a peak current of 2.7 kA will soon be performed. The high-power testing including a primary split pulse transformer will be also carried out to study the modulator performance. We also plan to build a full prototype modulator which is capable of driving two 75 MW PPM-klystrons at 100 Hz repetition rate by 2002.

ACKNOWLEDGEMENTS

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